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1. A digital logic circuit for determining an output value based on a plurality of inputs values, comprising:

an *n*-level look-ahead network that converts the plurality of input values to a plurality of intermediate values;

a plurality of multiplexers each having a first and a second input port, an output port, and a control port, the plurality of multiplexers arranged to form a pipelined multiplexer loop having at least a first and a second stage, the first stage consisting of a first multiplexer, and the second stage consisting of a second and a third multiplexer, the pipelined multiplexer loop being coupled to the *n*-level look-ahead network;

a first communications link that couples the output port of the second multiplexer to the first input port of the first multiplexer;

a second communications link that couples the output port of the third multiplexer to the second input port of the first multiplexer;

a first feedback loop that couples the output port of the first multiplexer to the control port of the first multiplexer, the first feedback loop comprising a first delay device having a first delay time; and

a second feedback loop that couples the output port of the first multiplexer to the control ports of the second and third multiplexers, the second feedback loop comprising the first delay device and a second delay device having a second delay time,

wherein the first delay time is an integer multiple of the second delay time and is equal to (n+1) times a clock period of operation of the digital logic circuit.

2. The digital logic circuit of claim 1, wherein the *n*-level look-ahead network is a 2-level look-ahead network.

3. The digital logic circuit of claim 1, wherein each of the plurality of multiplexers is a 2-to-1 multiplexer.

4. The digital logic circuit of claim 1, wherein the digital logic circuit forms part of a computer processing system.

5. The digital logic circuit of claim 1, wherein the digital logic circuit forms part of a transceiver.

6. The digital logic circuit of claim 1, wherein the first delay time is nominally two times longer than the second delay time.

7. The digital logic circuit of claim 1, wherein the first delay device and the second delay device each comprise at least one data flip-flop.

8. The digital logic circuit of claim 1, wherein the digital logic circuit forms part of a communications system operating at a data rate of at least 3 gigabits per second.

9. The digital logic circuit of claim 1, wherein the digital logic circuit forms part of a decision feedback equalizer.

10. A digital logic circuit for determining an output value based on a plurality of inputs values, comprising:

an *n*-level look-ahead network that converts the plurality of input values to a plurality of intermediate values;

a plurality of multiplexers each having a first and a second input port, an output port, and a control port, the plurality of multiplexers arranged to form a pipelined multiplexer loop, the pipelined multiplexer loop being coupled to the *n*-level look-ahead network;

a first communications link that couples the output port of a first multiplexer to the first input port of a second multiplexer;

a second communications link that couples the output port of a third multiplexer to the second input port of the second multiplexer;

a first feedback loop that couples the output port of the second multiplexer to the control port of the second multiplexer, the first feedback loop comprising a first delay device having a first delay time; and

a second feedback loop that couples the output port of the second multiplexer to the control ports of the first and third multiplexers, the second feedback loop comprising the first delay device and a second delay device having a second delay time,

wherein the first delay time is an integer multiple of the second delay time and is equal to (n+1) times a clock period of operation of the digital logic circuit.

11. (ONCE AMENDED) The digital logic circuit of claim 10, wherein the digital logic circuit forms part of a transceiver.

12. (ONCE AMENDED) The digital logic circuit of claim 10, wherein the digital logic circuit forms part of a computer processing system.

13. (ONCE AMENDED) The digital logic circuit of claim 10, wherein the first delay device and the second delay device each comprise at least one data flip-flop.

14. (ONCE AMENDED) The digital logic circuit of claim 10, wherein the digital logic circuit forms part of a communications system operating at a data rate of at least 3 gigabits per second.

15. (ONCE AMENDED) The digital logic circuit of claim 10, wherein the digital logic circuit forms part of a decision feedback equalizer.

16. A method for pipelining multiplexer loops that form part of an integrated circuit, the method comprising the steps of:

(a) selecting a number of input values to be provided to a pipelined multiplexer loop during a clock period of operation of the integrated circuit;

(b) selecting a number of look-ahead steps to be implemented as a part of the pipelined multiplexer loop; and

(c) implementing the pipelined multiplexer loop using at least one digital logic circuit, comprising:

an *n*-level look-ahead network that converts the number of input values selected in step (1) to a plurality of intermediate values, wherein *n* represents the number of look-ahead steps selected in step (2),

a plurality of multiplexers each having a first and a second input port, an output port, and a control port, the plurality of multiplexers arranged to form the pipelined multiplexer loop, the pipelined multiplexer loop having at least a first and a second stage, the first stage consisting of a first multiplexer, and the second stage consisting of a second and a third multiplexer, the pipelined multiplexer loop being coupled to the *n*-level look-ahead network,

a first communications link that couples the output port of the second multiplexer to the first input port of the first multiplexer,

a second communications link that couples the output port of the third multiplexer to the second input port of the first multiplexer,

a first feedback loop, having a first delay time, that couples the output port of the first multiplexer to the control port of the first multiplexer, and

a second feedback loop, having a second delay time, that couples the output port of the first multiplexer to the control ports of the second and third multiplexers,

wherein the first delay time is an integer multiple of the second delay time and is equal to (n+1) times a clock period of operation of the integrated circuit.

17. The method of claim 16, wherein step (3) further comprising the step of:

implementing the pipelined multiplexer loop of the at least one digital logic circuit in a communications system.

18. The method of claim 16, wherein step (3) further comprising the step of:

implementing the pipelined multiplexer loop of the at least one digital logic circuit in a computer processing system.

19. The method of claim 16, further comprising the step of:

operating the pipelined multiplexer loop of the at least one digital logic circuit at a rate sufficient to process data at a rate equal to at least 3 gigabits per second.

20. The method of claim 16, further comprising the step of:

redistributing the first time delay and the second time delay using retiming techniques.